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Our Ref.: 9804-0015-999

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| Recipient: Examiner Allen C. Wong | Facsimile Number: (703) 872-9306 |
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Confirmation copy will not follow.

Re: U.S. Patent Application No. 09/517,804
Filing Date: March 2, 2000
Applicants: Amit Guilati et al.
Attorney Docket No. 9804-0015-999



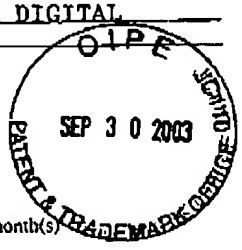
***Message***

Please see the attached response and return postcard as forwarded to the Patent Office on September 30, 2003.

Please contact me at your earliest convenience so that we can discuss this response.

Express Mail No. EV 313 841 855 US First Class Mail ( )
Date Mailed September 30, 2003
Serial No. 09/517,804 Filed 03/02/2000
Inventor GULATI et al.
For APPARATUS AND METHOD FOR SCALABLE BUFFERING IN A DIGITAL VIDEO DECODER

**DUE: 10/30/03**




( ) Affidavit/Declaration
( ) Amendment ( ) Response
( ) Application ____ pages
( ) ____ claims ____ drawing sheets
( ) Assignment ( ) Cover Sheet
(X) Brief (in triplicate)
( ) Declaration & Power of Attorney
  ( ) Executed ( ) Unexecuted ( ) Copy
( ) Declaration of Inventor(s)
  ( ) Executed ( ) Unexecuted ( ) Copy
( ) Design Application
( ) Disclaimer ( ) Disclaimer Fee
( ) Disclosure Statement ( ) Form PTO-1449
  ( ) w/refs. ( ) w/o refs.
( ) Drawings, Formal
  ____ Sheets ____ Figures

( ) Fee Address Indication Form
( ) Fee Calculation
( ) Issue Fee Transmittal
( ) Notice of Appeal
( ) Oral Hearing Request/Confirm
( ) Petition to Extend Time ____ month(s)
( ) Petition under 37 C.F.R. ____
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  ( ) by Assignee ( ) Associate ( ) with Revocation
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Other: Amendment After Final

File No. 9804-0015-999 Sender: GSW/bj

Express Mail No. EV 313 841 855 US

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: Gulati et al. | | Confirmation No.: | 4426 |
| Serial No.: | 09/517,804 | Art Unit: | 2613 |
| Filed: | March 2, 2000 | Examiner: | Wong, Allen C. |
| For: | *Apparatus and Method for Scalable Buffering in a Digital Video Decoder* | Attorney Docket No: | 9804-0015-999 |
| | | Date: | Sept. 30, 2003 |

AMENDMENT AFTER FINAL REJECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The enclosed Amendment is in response to the Final Office Action dated July 30, 2003 for the above identified patent application. This response is being filed within 2 months of the office action mailing date.

The Commissioner is hereby authorized to charge any required fee(s) to Pennie & Edmonds LLP Deposit Account No. 16-1150. A copy of this sheet is enclosed for such purpose.

IN THE CLAIMS:

Rewrite the claims as follows:

1. (Currently Amended) A method of assigning a buffer size in a video decoder, comprising:

establishing a first buffer size for a scalable buffer;

processing a video data stream with said scalable buffer configured to said first buffer size;

selecting a second buffer size for said scalable buffer;

processing said video data stream with said scalable buffer configured to said second buffer size;

creating memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and the processing with said scalable buffer configured to said second buffer size; and

assigning a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data;

wherein the memory utilization data includes cache miss rate data.

2. (Previously Amended) The method of claim 1 wherein said establishing and said selecting each include defining a buffer size as a multiple of a buffer size for storing a single macroblock.

3. (Previously Amended) The method of claim 1 wherein said processing includes utilizing said scalable buffer with a variable length decoder.

4. (Previously Amended) The method of claim 1 wherein said processing includes utilizing said scalable buffer with an inverse discrete cosine transfer function module.

5. (Previously Amended) The method of claim 1 wherein said processing includes utilizing said scalable buffer with a motion compensator.

6. (Previously Amended) The method of claim 1 wherein said creating includes creating cache utilization data defining data cache miss rates.

7. (Previously Amended) The method of claim 1 wherein said creating includes creating cache utilization data defining instruction cache miss rates.

8. (Previously Amended) The method of claim 1 further comprising modifying the size of video data stream processing instructions to correspond to said buffer size selected in said assigning step.

9. (Currently Amended) The method of claim 8 wherein said modifying includes loop unrolling video data stream processing instructions to correspond to said buffer size selected in said assigning step.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) A computer readable memory to direct a computer to function in a specified manner, comprising:

a buffer management module to establish a first buffer size and a second buffer size for a scalable buffer;

a video decoding module to process a video stream with said scalable buffer configured to said first buffer size and then said second buffer size; and

an analysis module to create memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and during the processing with said scalable buffer configured to said second buffer size, said analysis module including a buffer size adjuster to assign a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data;

wherein the memory utilization data includes cache miss rate data.

14. (Previously Amended) The computer readable memory of claim 13 wherein said buffer management module establishes said first buffer size as a first multiple of a buffer size for storing a single macroblock and said second buffer size as a second multiple of a buffer size for storing a single macroblock.

15. (Cancelled)

16. (Original) The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a variable length decoder.

17. (Original) The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with an inverse discrete cosine transfer function module.

18. (Original) The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a motion compensator.

19. (Original) The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining data cache miss rates.

20. (Original) The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining instruction cache miss rates.

21. (Previously Added) The computer readable memory of claim 13 wherein said analysis module further includes a subsystem to modify the size of video data stream processing instructions to correspond to said buffer size assigned by the buffer size adjuster.

22. (Currently Added) The computer readable memory of claim 21 wherein said subsystem performs loop unrolling of video data stream processing instructions to correspond to said buffer size assigned by the buffer size adjuster.

## REMARKS

This amendment responds to the final office action mailed July 30, 2003. In the office action the Examiner:

- rejected claims 1-9, 13, 14 and 16-22 under 35 U.S.C. 103(a) as being unpatentable over Cheney (U.S. Patent No. 5,668,599) in view of Orbits (U.S. Patent No. 5,630,097).

### Claim Amendments

With this amendment, Applicants have amended claims 1 and 13 to recite that the buffer size assigned to the scalable buffer is dependent upon the first and second buffer sizes chosen by the buffer management module. Support for such amendment can be found in Fig. 5 and page 13, lines 3-9. Claims 9 and 22 have been amended for clarity. No new subject matter has been added. After entry of this amendment, the pending claims are: claims 1-9, 13, 14 and 16-22.

### The rejections under 35 U.S.C. 103 should be withdrawn

The Examiner has rejected claims 1-9, 13, 14 and 16-22 under 35 U.S.C. 103(a) as being unpatentable over Cheney in view of Orbits. Applicants respectfully traverse the rejection.

To reject claims in an application under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). In order to establish prima facie obviousness, the prior art, either alone or in combination, must teach or suggest each limitation of the rejected claims. See *In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991); *In re Royka and Martin* 180 USPQ 580 (C.C.P.A. 1974); and *In re Wilson* 165 USPQ 494 (C.C.P.A. 1970). In the present instance, the cited arts fail to teach or suggest each limitation of the rejected claims.

Claim 13 is directed to a computer readable memory that directs a computer to function in a specified manner. The memory comprises a buffer management module to establish a buffer size for a scalable buffer and an analysis module to monitor the computer's cache memory performance when the scalable buffer is configured to the buffer size.

More specifically, the buffer management module establishes a first buffer size for the scalable buffer. In response, the analysis module analyzes the computer's cache memory performance and creates corresponding memory utilization data characterizing the cache memory performance. After that, the buffer management module establishes a second buffer

size for the scalable buffer, and the analysis module analyzes the computer's cache memory performance once again and creates corresponding memory utilization data. Through analyzing the memory utilization data in connection with the first and second buffer sizes, the analysis module selects an optimal buffer size to achieve low overall cache miss rate when the scalable buffer is configured to the optimal buffer size.

In other words, determining the optimal buffer size is a trial-and-error process. The variation of the overall cache miss rate is best characterized as a curve shown in Fig. 4c. To select an optimal buffer size, the analysis module needs to locate the bottom 430 on the curve by estimating the cache miss rate at multiple buffer sizes, including the first and second buffer sizes. Therefore, the optimal buffer size can be regarded as a function of the first and second buffer sizes through the memory utilization data (page 7, lines 19-32).

Cheney, however, relates to a system that minimizes the usage of a main memory, not a cache memory, through the use of a Spill Buffer in the main memory. While the Spill Buffer size may change, it varies only in accordance with parameters such as the operation modes and the frame sizes (Figs. 12-15) and there is no relationship or dependency between one and another Spill Buffer size. In other words, given a set of video decoding and displaying parameters, the Spill Buffer size is completely determined. Since Cheney does not teach a method of determining an optimal buffer size in accordance with first and second buffer sizes, the Spill Buffer in Cheney is not equivalent to the scalable buffer in Applicants' invention.

Even though Orbits discloses a cache management routine that is applied for reducing the cache miss rate, Orbits does not disclose a scalable buffer and a method of assigning a buffer size to the scalable buffer as recited in claim 13. Although there is a buffer 42 in Orbits for recording the sampled bus activity when a counter 41 overflows, Orbits does not suggest the size of the buffer 42 is scalable at all (Fig. 5 and column 6, lines 43-52).

Since Cheney and Orbits, either alone or in combination, do not teach or suggest the use of a scalable buffer and the method of determining its size as recited in claim 13, claim 13 and its dependent claims 14 and 16-22 are patentable over Cheney in view of Orbits.

Claim 1 is a method claim that has similar elements as claim 13. Therefore, claim 1 and its dependent claims 2-9 are also patentable over Cheney in view of Orbits.

In addition, claims 8 and 21 recite that the size of video data stream processing instructions is modified according to the buffer size selected by the analysis module, and

claims 9 and 22 further recite that the video data stream processing instructions are loop unrolled to match the buffer size selected by the analysis module.

Cheney, however, teaches the adjustment of a spill buffer to store picture data of different sizes, not video data stream processing instructions. The picture data of Cheney is different from video data stream processing instructions of claims 8, 9, 21, 22, as demonstrated by the fact that loop unrolling would not make sense with respect to picture data.

In light of the above amendments and remarks, Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at 650-849-7721, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 30, 2003

31,066
(Reg. No.)

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